What is claimed is:

1   1.   In an integrated circuit wireless communication device, a method for

2   Viterbi decoding comprising:

3   receiving a transmitted signal over a channel substantially characterized by a

4   scalar gain value and a noise value;

5   processing the gain value and noise value to determine a branch metric by

6   determining a log of the scalar gain value and subtracting therefrom a log of the noise

7   value and subtracting therefrom the log of a first constant to form a first sum, and

8   determining an antilog of the first sum and subtracting therefrom a second constant to

9   form a second sum, the second sum corresponding to the branch metric; and

10   providing the branch metric to a Viterbi decoder.

1   2.   The method of claim 1, wherein the processing of the gain value and noise

2   value to determine a branch metric scaling further comprises adding a log of a location

3   information scaling factor to the first sum.

1   3.   The method of claim 1, wherein the processing of the gain value and noise

2   value to determine a branch metric further comprises rounding out any fractional bits in

3   the second sum.

1   4.   The method of claim 1, wherein the processing of the gain value and noise

2   value to determine a branch metric further comprises saturating the second sum.

1   5.   The method of claim 1, wherein the processing of the gain value and noise

2   value to determine a branch metric further comprises using a processor to calculate a

3   branch metric (M) using the equation $M = \left\lceil \dfrac{1}{C_1} \dfrac{|H|^2 k_{loc}^2}{\sigma^2} - C_2 \right\rceil$.

1   6.   The method of claim 1, wherein the log of the scalar gain value is

2   determined by:

3   determining a lower integer boundary L for the scalar gain value which is a bit

4   position of a most significant "1" in a binary representation of the scalar gain value;

5   interpolating an interpolated value between L and L+1 using a lookup table

6   indexed by P next most significant bits of the scalar gain value; and

7   concatenating the lower integer boundary L and the interpolated value to form the

8   log of the scalar gain value.

1   7.   The method of claim 6, wherein the determination of a lower integer

2   boundary L comprises left shifting the scalar gain value a required number of shifts until

3   an N-1 bit position contains a one value, and then subtracting the required number of

4   shifts from the N-1 value.

1   8.   The method of claim 1, wherein the log of the noise value is determined

2   by:

3   determining a first value which is a bit position of the most significant "1" in an

4   N-bit binary representation of the noise value;

5   determining a second value by interpolating between the first value and the first

6   value plus one using a lookup table; and

7   concatenating the first value and the second value as a most significant bits

8   portion and least significant bits portion, respectively, to form the log of the noise value.

1   9.   The method of claim 1, wherein the antilog of the first sum is determined

2   by:

3   right shifting the first sum by R bits to generate a left shift control signal; and

4   using the R least significant bits of the first sum as an index into a lookup table to

5   generate an intermediate value which is left shifted under control of the left shift control

6   signal to generate the antilog of the first sum.

1   10.   The method of claim 1, wherein the processing of the gain value and noise

2   value are performed by a PHY module in a wireless interface device.

1   11.   An article of manufacture having at least one recordable medium having

2   stored thereon executable instructions and data which, when executed by at least one

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3   processing device, cause the at least one processing device to compute a branch metric

4   for a Viterbi decoder, comprising implementing a multiplication operation of a first term

5   and a second term in the branch metric computation by:

6   adding a log of the first term to a log of the second term to form a first sum; and

7   determining the antilog of the first sum.

1   12.   The article of manufacture of claim 11, wherein the processing device

2   computes a branch metric for a Viterbi decoder by

3   computing a $\log_2|H|^2$ value, where H represents a scalar gain value for a

4   transmission channel;

5   subtracting a $\log_2\sigma^2$ value from the $\log_2|H|^2$ value to form a first sum, where σ^2

6   represents the a noise variance value for the transmission channel;

7   subtracting a $\log_2 C_1$ value from the first sum to form a second sum, where the C_1

8   value has been pre-computed and stored in memory;

9   computing an antilog of the second sum; and

10   subtracting a C_2 value which has been stored in memory from the antilog of the

11   second sum to form a branch metric.

1   13.   The article of manufacture of claim 12, wherein processing device rounds

2   out any fractional bits in the branch metric and saturates the branch metric to a

3   predetermined range.

1   14.   An apparatus for decoding a signal, the apparatus comprising:

2   means for receiving a sampled signal;

3   means for demapping the received sampled signal into a branch metric

4   comprising means for performing multiplication operations in a log domain using an

5   adder circuit and means for performing division operations in a log domain using an

6   subtractor circuit; and

7   means for providing the branch metric a Viterbi decoder.

1   15.   The apparatus of claim 14, where the means for demapping comprises a

2   means for calculating a log function.

1   16.   The apparatus of claim 14, where the means for demapping comprises a

2   means for calculating an antilog function.

1   17.   The apparatus of claim 14, where the means for demapping comprises a

2   means for calculating a branch metric (M) using the equation $M = \left\lceil \dfrac{1}{C_1} \dfrac{|H|^2 k_{loc}^2}{\sigma^2} - C_2 \right\rceil$.

1   18.   The apparatus of claim 14, where the means for demapping comprises a

2   means for calculating a branch metric (M) using the equation $M = \left\lceil \dfrac{1}{C_1} \dfrac{|H|^2}{\sigma^2} - C_2 \right\rceil$.

1   19.   The apparatus of claim 14, where the means for demapping comprises

2   an input for accepting a first value representing the scalar gain for a transmission

3   channel;

4   a log unit that accepts the first value from the input and determines a log of the

5   first value;

6   a first subtractor for subtracting a log of a second value from the log of the first

7   value to form a first difference, said second value representing a measure of additive

8   white Gaussian noise for a channel over which the sampled signal was transmitted;

9   a second subtractor for subtracting a log of a first constant from the first

10   difference to form a second difference;

11   a first adder for adding a log of a location information scaling factor (k_{loc}) to the

12   second difference to form a first sum;

13   an antilog unit that accepts the first sum and determines an antilog of the first

14   sum;

15   a second adder for adding the antilog of the first sum to a second constant to a

16   preliminary branch metric, where the second constant comprises an offset that is a

17   function of a transmit constellation for the transmit channel; and

18   a saturation unit for saturating the preliminary branch metric to generate the

19   branch metric.

1   20.   The apparatus of claim 19, wherein the first subtractor and second

2   subtractor are implemented as a single circuit.